AC '97 SoundMAX® Codec

AD1981BL

AC '97 2.3 COMPATIBLE FEATURES

- S/PDIF output, 20-bit data format, supporting 48 kHz and 44.1 kHz sample rates
- Integrated stereo headphone amplifier
- Variable sample rate audio
- External audio power-down control
- >90 dB dynamic range
- Stereo full-duplex codec
- 20-bit PCM DAC
- 3 analog line-level stereo inputs for line-in, AUX, and CD
- Mono line-level phone input
- Dual MIC input with built-in programmable preamplifier
- High quality CD input with ground sense
- Mono output for speakerphone or internal speaker power management support
- 48-lead LQFP package, Pb-free available

ENHANCED FEATURES

- Stereo MIC preamplifier support
- Built-in digital equalizer function for optimized speaker sound
- Full-duplex variable sample rates from 7040 Hz to 48 kHz with 1 Hz resolution
- Jack sense pins for automatic output switching
- Software-programmed V_{REFOUT} output for biasing microphone and external power amplifier
- Low power 3.3 V operation for analog and digital supplies
- Multiple codec configuration options

FUNCTIONAL BLOCK DIAGRAM

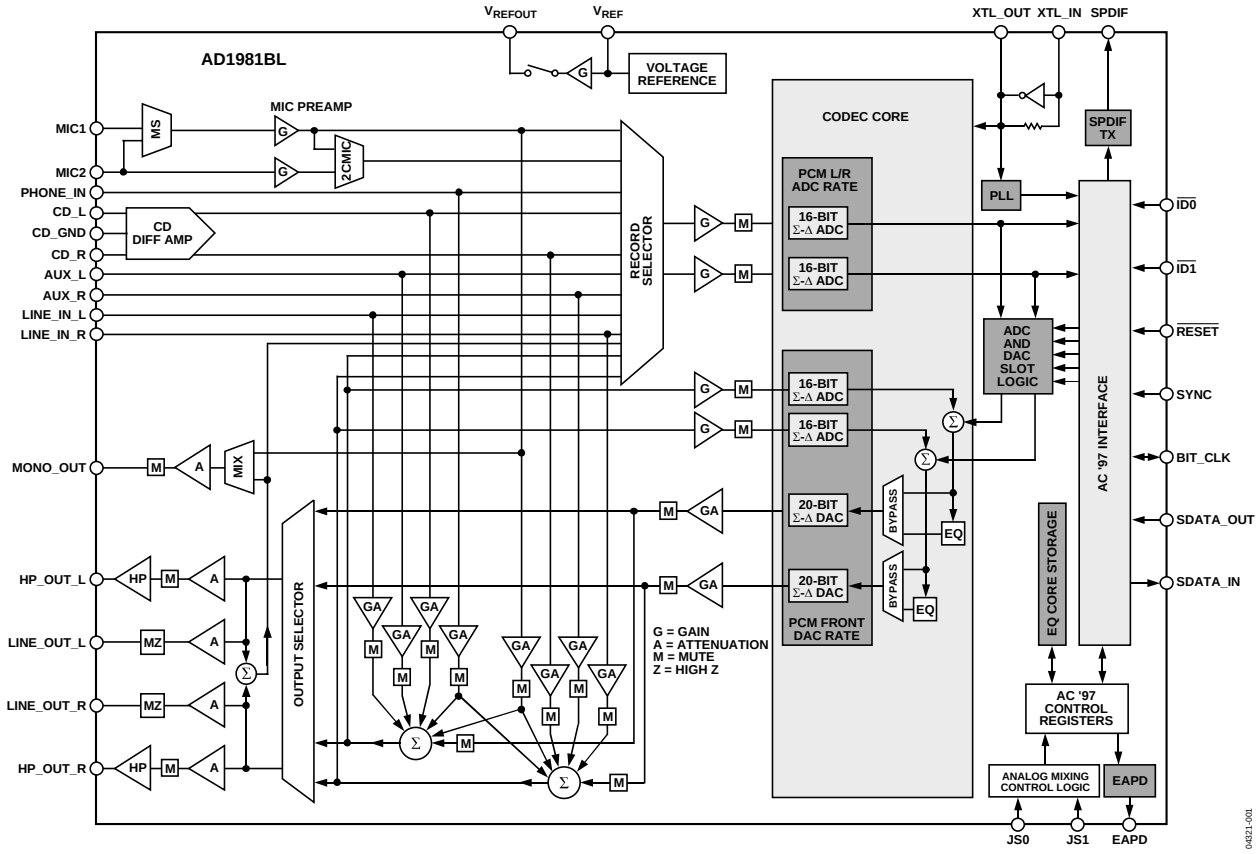


Figure 1.

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.326.8703

TABLE OF CONTENTS

REVISION HISTORY

1/05—Rev. 0 to Rev. A

Updated Format ... Universal
Changes to Ordering Guide ... 32

1/04—Revision 0: Initial Version

SPECIFICATIONS

TEST CONDITIONS

Standard test conditions, unless otherwise noted.

Table 1.

Parameter	Test Condition
Temperature	25°C
Digital Supply (DV_{DD})	3.3 V
Analog Supply (AV_{DD})	3.3 V
Sample Rate (f_S)	48 kHz
Input Signal	1008 Hz
Analog Output Pass Band	20 Hz to 20 kHz
DAC	Calibrated
	−3 dB Attenuation Relative to Full Scale
	0 dB Input
	10 kΩ Output Load (LINE_OUT)
	32 Ω Output Load (HP_OUT)
ADC	Calibrated
	0 dB Gain
	Input −3.0 dB Relative to Full Scale

GENERAL SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit
ANALOG INPUT				
Input Voltage (RMS Values Assume Sine Wave Input)				
LINE_IN, AUX, CD, PHONE_IN		0.707		V rms
		2.0		V p-p
MIC_IN with 20 dB Gain		0.0707		V rms
		0.2		V p-p
MIC_IN with 0 dB Gain		1.707		V rms
		2.0		V p-p
Input Impedance[1]		20		kΩ
Input Capacitance[1]		5	7.5	pF
MASTER VOLUME				
Step Size (0 dB to −46.5 dB): LINE_OUT_L, LINE_OUT_R		1.5		dB
Output Attenuation Range[1]		46.5		dB
Step Size (0 dB to −46.5 dB): MONO_OUT		1.5		dB
Output Attenuation Range[1]		46.5		dB
Step Size (0 dB to −46.5 dB): HP_OUT_R, HP_OUT_L		1.5		dB
Output Attenuation Range Span[1]		46.5		dB
Mute Attenuation of 0 dB Fundamental[1]	80			dB
PROGRAMMABLE GAIN AMPLIFIER—ADC				
Step Size (0 dB to 22.5 dB)		1.5		dB
PGA Gain Range		22.5		dB
ANALOG MIXER—INPUT GAIN/AMPLIFIERS/ATTENUATORS				
Signal-to-Noise Ratio (SNR)				
CD to LINE_OUT		90		dB
Other to LINE_OUT[1]		90		dB

Parameter	Min	Typ	Max	Unit
Step Size (+12 dB to −34.5 dB) (All Steps Tested):				
MIC_IN, LINE_IN, CD, AUX, PHONE_IN, DAC		1.5		dB
Input Gain/Attenuation Range:				
MIC_IN, LINE_IN, CD, AUX, PHONE_IN, DAC		46.5		dB
DIGITAL DECIMATION AND INTERPOLATION FILTERS[1]				
Pass Band	0		$0.4 \times f_S$	Hz
Pass-Band Ripple			±0.09	dB
Transition Band	$0.4 \times f_S$		$0.6 \times f_S$	Hz
Stop Band	$0.6 \times f_S$		∞	Hz
Stop-Band Rejection	−74			dB
Group Delay		$16/f_S$		sec
Group Delay Variation over Pass Band		0		µs
ANALOG-TO-DIGITAL CONVERTERS				
Resolution		16		Bits
Total Harmonic Distortion (THD)		−87		dB
Dynamic Range (−60 dB Input THD + N Referenced to Full Scale, A-Weighted)	78	83		dB
Signal-to-Intermodulation Distortion[1]CCIF Method)		85		dB
ADC Crosstalk[1]				
Line Inputs (Input L, Ground R, Read R; Input R, Ground L, Read L)		−80		dB
Line_In to Other		−100	−80	dB
Gain Error[2] (Full-Scale Span Relative to Nominal Input Voltage)			±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)			± 0.5	dB
ADC Offset Error[1]			±5	mV
DIGITAL-TO-ANALOG CONVERTERS				
Resolution		20		Bits
Total Harmonic Distortion (THD) LINE_OUT		−88		dB
Total Harmonic Distortion (THD) HP_OUT		−81		dB
Dynamic Range (−60 dB Input THD + N Referenced to Full Scale, A-Weighted)	82	87.5		dB
Signal-to-Intermodulation Distortion[1] (CCIF Method)		−100		dB
Gain Error[2] (Output FS Voltage Relative to Nominal Output FS Voltage)			±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.7	dB
DAC Crosstalk[1] (Input L, Zero R, Measure R_OUT; Input R, Zero L, Measure L_OUT)			−80	dB
ANALOG OUTPUT				
Full-Scale Output Voltage; LINE_OUT and MONO_OUT		0.707		V rms
		2.0		V p-p
Output Impedance[1]			800	Ω
External Load Impedance[1]	10			kΩ
Output Capacitance[1]		15		pF
External Load Capacitance[1]			100	pF
Full-Scale Output Voltage; HP_OUT (0 dB Gain)		1		V rms
External Load Impedance[1]	32			Ω
V_{REF}	1	1.12	1.225	V
V_{REFOUT}		2.25		V
V_{REFOUT} Current Drive			5	mA
Mute Click (Muted Output Minus Unmuted Midscale DAC Output)		±5		mV
STATIC DIGITAL SPECIFICATIONS				
High Level Input Voltage (V_{IH}): Digital Inputs	$0.65 \times DV_{DD}$			V
Low Level Input Voltage (V_{IL})			$0.35 \times DV_{DD}$	V
High Level Output Voltage (V_{OH}), I_{OH} = 2 mA	$0.9 \times DV_{DD}$			V

Parameter	Min	Typ	Max	Unit
Low Level Output Voltage (V_{OL}), I_{OL} = 2 mA			0.1 × DV_{DD}	V
Input Leakage Current	−10		+10	µA
Output Leakage Current	−10		+10	µA
POWER SUPPLY				
Power Supply Range (AV_{DD} and DV_{DD})	3.0		3.47	V
Power Dissipation		2.87		mW
Analog Supply Current—3.3 V (AV_{DD})		39		mA
Digital Supply Current—3.3 V (DV_{DD})		48		mA
Power Supply Rejection (100 mV p-p Signal at 1 kHz)[1] (At Both Analog and Digital Supply Pins, Both ADCs and DACs)		40		dB
CLOCK SPECIFICATIONS[1]				
Input Clock Frequency		24.576		MHz
Recommended Clock Duty Cycle	40	50	60	%

[1] Guaranteed but not tested.
[2] Measurements reflect main ADC.

POWER-DOWN STATES

Values presented with V_{REFOUT} not loaded.

Table 3.

Parameter	Set Bits	DV_{DD} Typ	AV_{DD} Typ	Unit
Fully Active	No Bits Value	47.76	38.9	mA
ADC	PR0	40.1	34.39	mA
DAC	PR1	32.8	26.3	mA
ADC + DAC	PR1, PR0	13.2	20.55	mA
Mixer	PR2	47.7	19.39	mA
ADC + Mixer	PR2, PR0	40	14.86	mA
DAC + Mixer	PR2, PR1	32.77	6.39	mA
ADC + DAC + Mixer	PR2, PR1, PR0	13.9	1.15	mA
Standby	PR5, PR4, PR3, PR2, PR1, PR0	0	0	mA
Headphone Standby	PR6	47.7	32	mA

TIMING PARAMETERS

Guaranteed over operating temperature range.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{RESET}}$ Active Low Pulse Width	t_{RST_LOW}		1.0		ms
$\overline{\text{RESET}}$ Inactive to BIT_CLK Start-Up Delay	$t_{RST2CLK}$	162.8			ns
SYNC Active High Pulse Width	t_{SYNC_HIGH}		1.3		µs
SYNC Low Pulse Width	t_{SYNC_LOW}		19.5		µs
SYNC Inactive to BIT_CLK Start-Up Delay	$t_{SYNC2CLK}$	162.8			ns
BIT_CLK Frequency			12.288		MHz
BIT_CLK Frequency Accuracy				±1	ppm
BIT_CLK Period	t_{CLK_PERIOD}		81.4		ns
BIT_CLK Output Jitter[1, 2, 3]			750	2000	ps
BIT_CLK High Pulse Width	t_{CLK_HIGH}	32.56	42	48.84	ns
BIT_CLK Low Pulse Width	t_{CLK_LOW}	32.56	38		ns
SYNC Frequency			48.0		kHz

Parameter	Symbol	Min	Typ	Max	Unit
SYNC Period	t_{SYNC_PERIOD}		20.8		ms
Setup to Falling Edge of BIT_CLK	t_{SETUP}	5	2.5		ns
Hold from Falling Edge of BIT_CLK	t_{HOLD}	5			ns
BIT_CLK Rise Time	$t_{RISECLK}$	2	4	6	ns
BIT_CLK Fall Time	$t_{FALLCLK}$	2	4	6	ns
SYNC Rise Time	$t_{RISESYNC}$	2	4	6	ns
SYNC Fall Time	$t_{FALLSYNC}$	2	4	6	ns
SDATA_IN Rise Time	$t_{RISEDIN}$	2	4	6	ns
SDATA_IN Fall Time	$t_{FALLDIN}$	2	4	6	ns
SDATA_OUT Rise Time	$t_{RISEDOUT}$	2	4	6	ns
SDATA_OUT Fall Time	$t_{FALLDOUT}$	2	4	6	ns
End of Slot 2 to BIT_CLK, SDATA_IN Low	t_{S2_PDOWN}	0		1.0	ms
Setup to Trailing Edge of $\overline{\text{RESET}}$ (Applies to SYNC, SDATA_OUT)	$t_{SETUP2RST}$	15			ns
Rising Edge of $\overline{\text{RESET}}$ to High Z Delay	t_{OFF}			25	ns
Propagation Delay				15	ns
$\overline{\text{RESET}}$ Rise Time				50	ns
Output Valid Delay from Rising Edge of BIT_CLK to SDI Valid				15	ns

[1] Guaranteed but not tested.
[2] Output jitter is directly dependent on crystal input jitter.
[3] Maximum jitter specification is for noncrystal operation only. Crystal operation maximum is much lower.

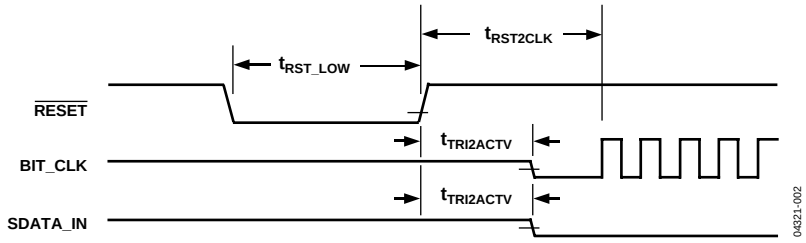


Figure 2. Cold Reset Timing (Codec is Supplying the BIT_CLK Signal)

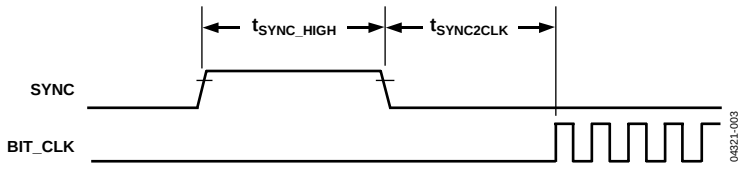


Figure 3. Warm Reset Timing

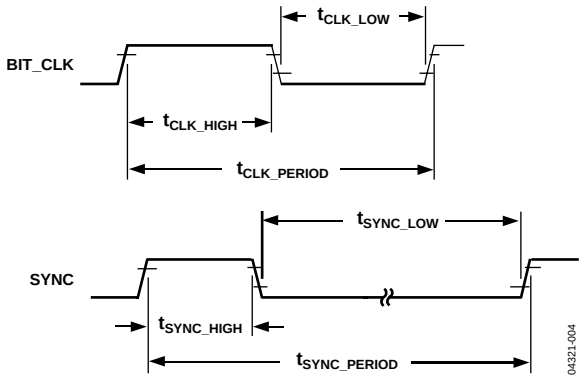


Figure 4. Clock Timing

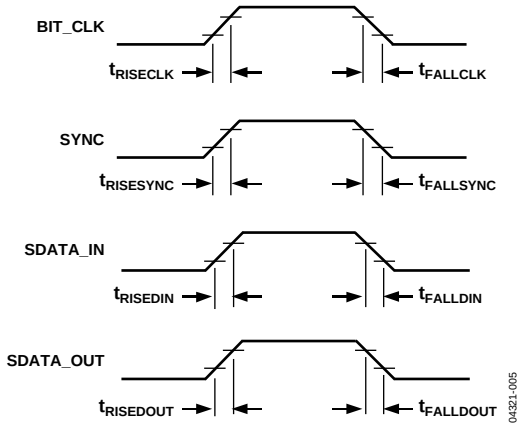


Figure 5. Signal Rise and Fall Times

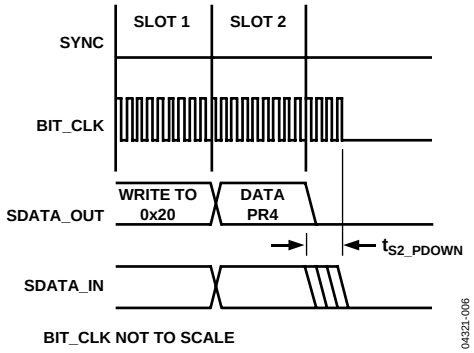


Figure 6. AC-Link Low Power Mode Timing

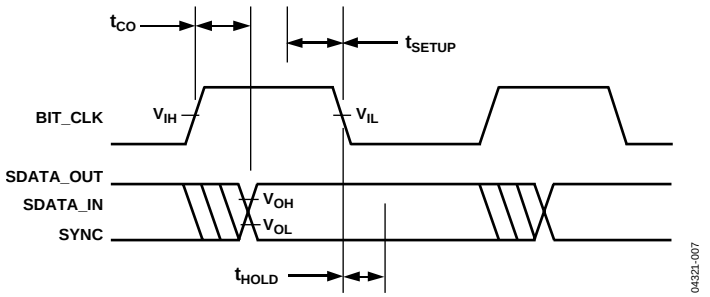


Figure 7. AC-Link Low Power Mode Timing, SYNC and BIT_CLK Chopped

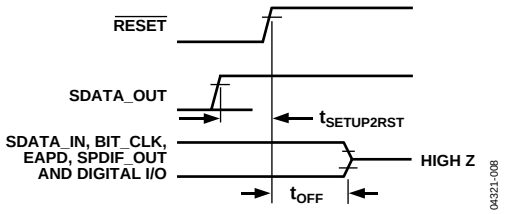


Figure 8. ATE Test Mode

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
Power Supplies	
Digital (DV_{DD})	−0.3 V to +3.6 V
Analog (AV_{DD})	−0.3 V to +6.0 V
Input Current (Except Supply Pins)	±10 mA
Signals Pins	
Digital Input Voltage	−0.3 V to DV_{DD} + 0.3 V
Analog Input Voltage	−0.3 V to AV_{DD} + 0.3 V
Ambient Temperature Range (Operating)	0°C to 70°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating (LQFP Package)
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W
θ_{JA} Thermal Resistance (Junction to Ambient)
θ_{JC} Thermal Resistance (Junction to Case)

Table 6. Thermal Resistance

Package	θ_{JA}	θ_{JC}
LQFP	50.1°C/W	17.8°C/W

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

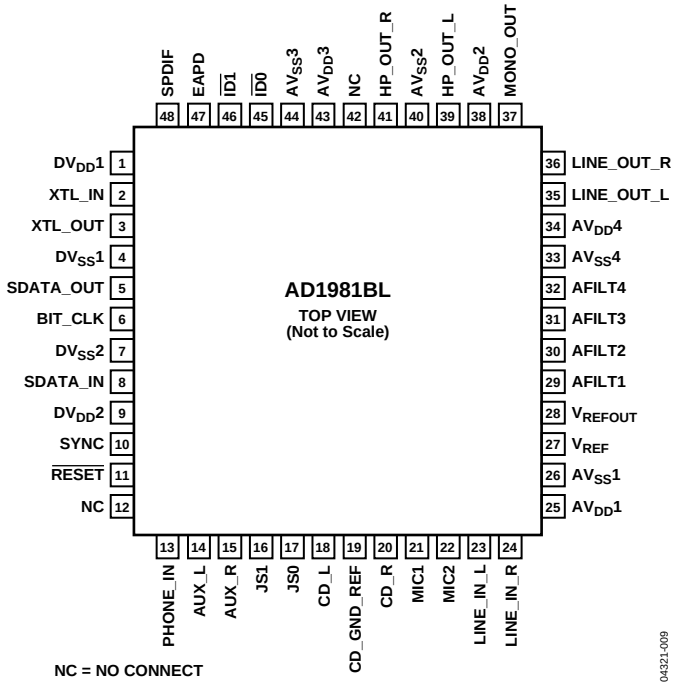


Figure 9. 48-Lead LQFP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	I/O	Description
DIGITAL I/O			
2	XTL_IN	I	Crystal Input (24.576 MHz) or External Clock Input.
3	XTL_OUT	O	Crystal Output.
5	SDATA_OUT	I	AC-Link Serial Data Output, AD1981BL Data Input Stream.
6	BIT_CLK	O/I	AC-Link Bit Clock Output (12.288 MHz) or Bit Clock Input, if Secondary Mode Selected.
8	SDATA_IN	O	AC-Link Serial Data Input, AD1981BL Data Output Stream.
10	SYNC	I	AC-Link Frame Sync.
11	$\overline{\text{RESET}}$	I	AC-Link Reset, AD1981BL Master Hardware Reset.
48	SPDIF	O	S/PDIF Output.
CHIP SELECTS[1]			
45	$\overline{\text{ID0}}$	I	Chip Select Input 0 (Active Low). This pin can also be used as the chain input from a secondary codec.
46	$\overline{\text{ID1}}$	I	Chip Select Input 1 (Active Low).
JACK SENSE AND EAPD			
17	JS0	I	Jack Sense 0 Input.
16	JS1	I	Jack Sense 1 Input.
47	EAPD	O	External Amp Power-Down Control.
ANALOG I/O			
13	PHONE_IN	I	Phone Input. Mono input from telephony subsystem speaker phone or handset.
14	AUX_L	I	Auxiliary Input Left Channel.
15	AUX_R	I	Auxiliary Input Right Channel.
18	CD_L	I	CD Audio Left Channel.
19	CD_GND_REF	I	CD Audio Analog Ground Reference for Differential CD Input.
20	CD_ R	I	CD Audio Right Channel.
21	MIC1	I	Microphone 1 Input (Mono) or Left Channel when 2-Channel Mode Selected (Stereo MIC).

Pin No.	Mnemonic	I/O	Description
22	MIC2	I	Microphone 2 Input (Mono) or Right Channel when 2-Channel Mode Selected (Stereo MIC).
23	LINE_IN_L	I	Line-In Left Channel.
24	LINE_IN_R	I	Line-In Right Channel.
35	LINE_OUT_L	O	Line-Out (Front) Left Channel.
36	LINE_OUT_R	O	Line-Out (Front) Right Channel.
37	MONO_OUT	O	Monaural Output to Telephony Subsystem Speaker Phone.
39	HP_OUT_L	O	Headphone Left-Channel Output.
41	HP_OUT_R	O	Headphone Right-Channel Output.
FILTER/REFERENCE[2]			
27	V_{REF}	O	Voltage Reference Filter.
28	V_{REFOUT}	O	Voltage Reference Output 5 mA Drive (Intended for MIC Bias and Power Amp Bias).
29	AFILT1	O	Antialiasing Filter Capacitor—ADC Right Channel.
30	AFILT2	O	Antialiasing Filter Capacitor—ADC Left Channel.
31	AFILT3	O	Antialiasing Filter Capacitor—Mixer ADC Right Channel.
32	AFILT4	O	Antialiasing Filter Capacitor—Mixer ADC Left Channel.
POWER AND GROUND SIGNALS			
1	$DV_{DD}1$	I	Digital V_{DD}, 3.3 V.
4	$DV_{SS}1$	I	Digital GND.
7	$DV_{SS}2$	I	Digital GND.
9	$DV_{DD}2$	I	Digital V_{DD}, 3.3 V.
25	$AV_{DD}1$	I	Analog V_{DD}, 3.3 V.
26	$AV_{SS}1$	I	Analog GND.
38	$AV_{DD}2$	I	Analog V_{DD}, 3.3 V.
40	$AV_{SS}2$	I	Analog GND.
43	$AV_{DD}3$	I	Analog V_{DD}, 3.3 V.
44	$AV_{SS}3$	I	Analog GND.
34	$AV_{DD}4$	I	Analog V_{DD}, 3.3 V.
33	$AV_{SS}4$	I	Analog GND.
NO CONNECTS			
12	NC		No Connect.
42	NC		No Connect.

[1] These pins can also be used to select an external clock. See Table 44.
[2] These signals are connected to resistors, capacitors, or specific voltages.

INDEXED CONTROL REGISTERS

Table 8.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x00	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	0x0090
0x02	Master Volume	MM	X	X	LMV4	LMV3	LMV2	LMV1	LMV0	RM[1]	X	X	RMV4	RMV3	RMV2	RMV1	RMV0	0x8000
0x04	Headphone Volume	HPM	X	X	LHV4	LHV3	LHV2	LHV1	LHV0	RM[1]	X	X	RHV4	RHV3	RHV2	RHV1	RHV0	0x8000
0x06	Mono Volume	MVM	X	X	X	X	X	X	X	X	X	X	MV4	MV3	MV2	MV1	MV0	0x8000
0x0C	Phone Volume	PHM	X	X	X	X	X	X	X	X	X	X	PHV4	PHV3	PHV2	PHV1	PHV0	0x8008
0x0E	MIC Volume	MCM	X	X	X	X	X	X	X	X	M20	X	MCV4	MCV3	MCV2	MCV1	MCV0	0x8008
0x10	Line-In Volume	LVM	X	X	LLV4	LLV3	LLV2	LLV1	LLV0	RM[1]	X	X	RLV4	RLV3	RLV2	RLV1	RLV0	0x8808
0x12	CD Volume	CVM	X	X	LCV4	LCV3	LCV2	LCV1	LCV0	RM[1]	X	X	RCV4	RCV3	RCV2	RCV1	RCV0	0x8808
0x16	AUX Volume	AM	X	X	LAV4	LAV3	LAV2	LAV1	LAV0	RM[1]	X	X	RAV4	RAV3	RAV2	RAV1	RAV0	0x8808
0x18	PCM-Out Volume	OM	X	X	LOV4	LOV3	LOV2	LOV1	LOV0	RM[1]	X	X	ROV4	ROV3	ROV2	ROV1	ROV0	0x8808
0x1A	Record Select	X	X	X	X	X	LS2	LS1	LS0	X	X	X	X	X	RS2	RS1	RS0	0x0000
0x1C	Record Gain	IM	X	X	X	LIM3	LIM2	LIM1	LIM0	RM[1]	X	X	X	RIM3	RIM2	RIM1	RIM0	0x8000
0x20	General-Purpose	X	X	X	X	X	X	MIX	MS	LPBK	X	X	X	X	X	X	X	0x0000
0x26	Power-Down Ctrl/Stat	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	0x000X
0x28	Ext'd Audio ID	IDC1	IDC0	X	X	REVC1	REVC0	AMAP	X	X	X	DSA1	DSA0	X	SPDIF	X	VRAS	0xX605
0x2A	Ext'd Audio Stat/Ctrl	VFORCE	X	X	X	X	SPCV	X	X	X	X	SPSA1	SPSA0	X	SPDIF	X	VRA	0x0000
0x2C	PCM Front DAC Rate	SRF15	SRF14	SRF13	SRF12	SRF11	SRF10	SRF9	SRF8	SRF7	SRF6	SRF5	SRF4	SRF3	SRF2	SRF1	SRF0	0xBB80
0x32	PCM L/R ADC Rate	SRA15	SRA14	SRA13	SRA12	SRA11	SRA10	SRA9	SRA8	SRA7	SRA6	SRA5	SRA4	SRA3	SRA2	SRA1	SRA0	0xBB80
0x3A	SPDIF Control	V	X	SPSR1	SPSR0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	/AUD	PRO	0x2000
0x60	EQ Ctrl	EQM	MAD LBEN	X	X	X	X	X	X	SYM	CHS	BCA5	BCA4	BCA3	BCA2	BCA1	BCA0	0x8080
0x62	EQ Data	CFD15	CFD14	CFD13	CFD12	CFD11	CFD10	CFD9	CFD8	CFD7	CFD6	CFD5	CFD4	CFD3	CFD2	CFD1	CFD0	0x0000
0x64	Mixer ADC, Volume	MXM	X	X	X	LMG3	LMG2	LMG1	LMG0	RM[1]	X	X	X	RMG3	RMG2	RMG1	RMG0	0x8000
0x72	Jack Sense	X	X	X	JS MT2	JS MT1	JS MT0	JS1 EQB	JS0 EQB	JS1 TMR	JS0 TMR	JS1 MD	JS0 MD	JS1 ST	JS0 ST	JS1 INT	JS0 INT	0x0000
0x74	Serial Config	SLOT 16	REGM 2	REGM 1	REGM 0	X	X	X	CHEN	X	X	X	INTS	X	SPAL	SPDZ	SPLNK	0x7001
0x76	Misc Control Bit	DACZ	X	MSPLT	LODIS	DAM	X	FMXE	X	MAD PD	2CMIC	X	MAD ST	VREFH	VREFD	MBG1	MBG0	0x0000
0x7C	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	0x4144
0x7E	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	0x5374

All registers are not shown. Bits containing an X are assumed to be reserved.
Odd register addresses are aliased to the next lower even address.
Reserved registers should not be written.
Zeros should be written to reserved bits.

[1] For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 0x76. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, the RM bit has no effect.

CONTROL REGISTER DETAILS

RESET REGISTER

Index 0x00

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x00	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	0x0090

X is a wild card, and has no effect on the value.
Writing any value to this register performs a register reset that causes all registers to revert to their default values (except 0x74, which forces the serial configuration).
Reading this register returns the ID code of the part and a code for the type of 3D stereo enhancement.

ID[9:0] Identify Capability. The ID decodes the capabilities of AD1981BL based on the functions listed in Table 9.

Table 9. ID Bits

Bit	Function	AD1981B
ID0	Dedicated MIC PCM in Channel	0
ID1	Modem Line Codec Support	0
ID2	Bass and Treble Control	0
ID3	Simulated Stereo (Mono to Stereo)	0
ID4	Headphone Out Support	1
ID5	Loudness (Bass Boost) Support	0
ID6	18-Bit DAC Resolution	0
ID7	20-Bit DAC Resolution	1
ID8	18-Bit ADC Resolution	0
ID9	20-Bit ADC Resolution	0

MASTER VOLUME REGISTER

Index 0x02

This register controls the Line_Out volume controls for both stereo channels and the mute bit. Each volume subregister contains five bits, generating 32 volume levels with 31 steps of 1.5 dB each. Because AC '97 defines 6-bit volume registers, to maintain compatibility whenever the D5 or D13 bits are set to 1, their respective lower five volume bits are automatically set to 1 by the codec logic. On readback, all lower five bits read 1s whenever these bits are set to 1. Refer to Table 12 for examples.

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x02	Master Volume	MM	X	X	LMV4	LMV3	LMV2	LMV1	LMV0	RM[1]	X	X	RMV4	RMV3	RMV2	RMV1	RMV0	0x8000

[1] For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 0x76. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, the RM bit has no effect.
All registers are not shown, and bits containing an X are assumed to be reserved.

Table 10.

Bit	Mnemonic	Function
RMV [4:0]	Right Master Volume Control	The least significant bit represents 1.5 dB. This register controls the output from 0 dB to a maximum attenuation of 46.5 dB.
RM	Right-Channel Mute	Once enabled by the MSPLT bit in Register 0x76, this bit mutes the right channel separately from the MM bit. Otherwise, this bit always reads 0 and has no effect when set to 1.
LMV [4:0]	Left Master Volume Control	The least significant bit represents 1.5 dB. This register controls the output from 0 dB to a maximum attenuation of 46.5 dB.
MM	Master Volume Mute	When this bit is set to 1, both the left and right channels are muted, unless the MSPLT bit in Register 0x76 is set to 1, in which case this mute bit affects only the left channel.

HEADPHONE VOLUME REGISTER

Index 0x04

This register controls the headphone volume controls for both stereo channels and the mute bit. Each volume subregister contains five bits, generating 32 volume levels with 31 steps of 1.5 dB each. Because AC '97 defines 6-bit volume registers, to maintain compatibility, whenever the D5 or D13 bits are set to 1, their respective lower five volume bits are automatically set to 1 by the codec logic. On readback, all lower five bits read 1s whenever these bits are set to 1. Refer to Table 12 for examples.

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x04	Headphone Volume	HPM	X	X	LHV4	LHV3	LHV2	LHV1	LHV0	RM[1]	X	X	RHV4	RHV3	RHV2	RHV1	RHV0	0x8000

[1] For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 0x76. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, the RM bit has no effect.

All registers are not shown, and bits containing an X are assumed to be reserved.

Table 11.

Bit	Mnemonic	Function
RHV [4:0]	Right Headphone Volume Control	The least significant bit represents 1.5 dB. This register controls the output from 0 dB to a maximum attenuation of 46.5 dB.
RM	Right-Channel Mute	Once enabled by the MSPLT bit in Register 0x76, this bit mutes the right channel separately from the HPM bit. Otherwise, this bit always reads 0 and has no effect when set to 1.
LHV [4:0]	Left Headphone Volume Control	The least significant bit represents 1.5 dB. This register controls the output from 0 dB to a maximum attenuation of 46.5 dB.
HPM	Headphone Volume Mute	When this bit is set to 1, both the left and right channels are muted, unless the MSPLT bit in Register 0x76 is set to 1, in which case this mute bit affects only the left channel.

Table 12. Volume Settings for Master and Headphone

Reg. 0x76	Control Bits Master Volume (0x02) and Headphone Volume (0x04)							
	Left-Channel Volume D [13:8]				Right-Channel Volume D [5:0]			
MSPLT[1]	D15	Write	Readback	Function	D7[1]	Write	Readback	Function
0	0	00 0000	00 0000	0 dB Gain	X	00 0000	00 0000	0 dB Gain
0	0	00 1111	00 1111	−22.5 dB Gain	X	00 1111	00 1111	−22.5 dB Gain
0	0	01 1111	01 1111	−46.5 dB Gain	X	01 1111	01 1111	−46.5 dB Gain
0	0	1X XXXX	01 1111	−46.5 dB Gain	X	1X XXXX	01 1111	−46.5 dB Gain
0	1	XX XXXX	XX XXXX	−∞ dB Gain, Muted	X	XX XXXX	XX XXXX	−∞ dB Gain, Muted
1	0	1X XXXX	01 1111	−46.5 dB Gain	1	XX XXXX	XX XXXX	−∞ dB Gain, Right Only Muted
1	1	XX XXXX	XX XXXX	−∞ dB Gain, Left Only Muted	0	XX XXXX	XX XXXX	−46.5 dB Gain
1	1	XX XXXX	XX XXXX	−∞ dB Gain, Left Muted	1	XX XXXX	XX XXXX	−∞ dB Gain, Right Muted

[1] For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 0x76. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, the RM bit has no effect.

X is a wild card, and has no effect on the value.

MONO VOLUME REGISTER

Index 0x06

This register controls the mono output volume and mute bit. The volume register contains five bits, generating 32 volume levels with 31 steps of 1.5 dB each. Because AC'97 defines 6-bit volume registers, to maintain compatibility, whenever the D5 bit is set to 1, their respective lower five volume bits are automatically set to 1 by the codec logic. On readback, all lower five bits read 1s whenever this bit is set to 1. Refer to Table 14 for examples.

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x06	Mono Volume	MVM	X	X	X	X	X	X	X	X	X	X	MV4	MV3	MV2	MV1	MV0	0x8000

All registers are not shown, and bits containing an X are assumed to be reserved.

Table 13.

Bit	Mnemonic	Function
MV [4:0]	Mono Volume Control	The least significant bit represents 1.5 dB. This register controls the output from 0 dB to a maximum attenuation of 46.5 dB.
MVM	Mono Volume Mute	When this bit is set to 1, the channel is muted.

Table 14. Volume Settings for Mono

	Control Bits D [4:0] for Mono (0x06)		
D15	Write	Readback	Function
0	0 0000	0 0000	0 dB Gain
0	0 1111	0 1111	−22.5 dB Gain
0	1 1111	1 1111	−46.5 dB Gain
1	X XXXX	X XXXX	−∞ dB Gain, Muted

An X is a wild card, and has no effect on the value.

PHONE VOLUME REGISTER

Index 0x0C

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x0C	Phone Volume	PHM	X	X	X	X	X	X	X	X	X	X	PHV4	PHV3	PHV2	PHV1	PHV0	0x8008

All registers are not shown, and bits containing an X are assumed to be reserved. Refer to Table 17 for examples.

Table 15.

Bit	Mnemonic	Function
PHV [4:0]	Phone Volume	Allows setting the phone volume attenuator in 32 volume levels with 31 steps of 1.5 dB each. The LSB represents 1.5 dB, and the gain range is +12 dB to −34.5 dB. The default value is 0 dB, with the mute bit enabled.
PHM	Phone Mute	When this bit is set to 1, the phone channel is muted.

All registers are not shown, and bits containing an X are assumed to be reserved. Refer to Table 17 for examples.

MIC VOLUME REGISTER
Index 0x0E

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x0E	MIC Volume	MCM	X	X	X	X	X	X	X	X	M20	X	MCV4	MCV3	MCV2	MCV1	MCV0	0x8008

All registers are not shown, and bits containing an X are assumed to be reserved. Refer to Table 17 for examples.

Table 16.

Bit	Mnemonic	Function
MCV [4:0]	MIC Volume Gain	Allows setting the phone volume attenuator in 32 volume levels with 31 steps of 1.5 dB each. The LSB represents 1.5 dB, and the gain range is +12 dB to −34.5 dB. The default value is 0 dB, with the mute bit enabled.
M20	MIC Gain Boost	This bit allows setting additional MIC gain to increase the microphone sensitivity. The nominal gain boost by default is 20 dB; however, Bits D0 and D1 (MBG [1:0]) on the miscellaneous control bits register (0x76) allow changing the gain boost to 10 dB or 30 dB, if necessary. 0 = Disabled; Gain = 0 dB 1 = Enabled; Default Gain = 20 dB (see Register 0x76, Bits D0, D1)
MCM	MIC Mute	When this bit is set to 1, the MIC channel is muted.

Table 17. Volume Settings for Phone and MIC

	Control Bits D [4:0] Phone (0x0C) and MIC (0x0E)		
D15	Write	Readback	Function
0	0 0000	0 0000	12 dB Gain
0	0 1000	0 1000	0 dB Gain
0	1 1111	1 1111	−34.5 dB Gain
1	X XXXX	X XXXX	−∞ db Gain, Muted

X is a wild card, and has no effect on the value.

LINE-IN VOLUME REGISTER
Index 0x10

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x10	Line-In Volume	LVM	X	X	LLV4	LLV3	LLV2	LLV1	LLV0	RM[1]	X	X	RLV4	RLV3	RLV2	RLV1	RLV0	0x8808

[1]For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 0x76. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, the RM bit has no effect.
All registers are not shown, and bits containing an X are assumed to be reserved. Refer to Table 22 for examples.

Table 18.

Bit	Mnemonic	Function
RLV [4:0]	Line-In Volume Right	Allows setting the line-in right-channel attenuator in 32 volume levels. The LSB represents 1.5 dB, and the range is +12 dB to −34.5 dB. The default value is 0 dB, mute enabled.
RM	Right-Channel Mute	Once enabled by the MSPLT bit in Register 0x76, this bit mutes the right channel separately from the LM bit. Otherwise, this bit always reads 0 and has no effect when set to 1.
LLV [4:0]	Line-In Volume Left	Allows setting the line-in left-channel attenuator in 32 volume levels. The LSB represents 1.5 dB, and the range is +12 dB to −34.5 dB. The default value is 0 dB, mute enabled.
LVM	Line-In Mute	When this bit is set to 1, both the left and right channels are muted, unless the MSPLT bit in Register 0x76 is set to 1, in which case this mute bit affects only the left channel.

CD VOLUME REGISTER
Index 0x12

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x12	CD Volume	CVM	X	X	LCV4	LCV3	LCV2	LCV1	LCV0	RM[1]	X	X	RCV4	RCV3	RCV2	RCV1	RCV0	0x8808

[1] For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 0x76. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, the RM bit has no effect.
All registers are not shown, and bits containing an X are assumed to be reserved. Refer to Table 22 for examples.

Table 19.

Bit	Mnemonic	Function
RCV [4:0]	Right CD Volume	Allows setting the CD right-channel attenuator in 32 volume levels. The LSB represents 1.5 dB, and the gain range is +12 dB to −34.5 dB. The default value is 0 dB, mute enabled.
RM	Right-Channel Mute	Once enabled by the MSPLT bit in Register 0x76, this bit mutes the right channel separately from the CVM bit. Otherwise, this bit always reads 0 and has no affect when set to 1.
LCV [4:0]	Left CD Volume	Allows setting the CD left-channel attenuator in 32 volume levels. The LSB represents 1.5 dB, and the gain range is +12 dB to −34.5 dB. The default value is 0 dB, mute enabled.
CVM	CD Volume Mute	When this bit is set to 1, both the left and right channels are muted, unless the MSPLT bit in Register 0x76 is set to 1, in which case this mute bit affects only the left channel.

AUX VOLUME REGISTER
Index 0x16

Reg No.	Name	D15	D14	D13	D12	D11	D1	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x16	AUX Volume	AM	X	X	LAV4	LAV3	LAV2	LAV1	LAV0	RM[1]	X	X	RAV4	RAV3	RAV2	RAV1	RAV0	0x8808

[1] For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 0x76. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, the RM bit has no effect.
All registers are not shown, and bits containing an X are assumed to be reserved. Refer to Table 22 for examples.

Table 20.

Bit	Mnemonic	Function
RAV [4:0]	Right AUX Volume	Allows setting the AUX right-channel attenuator in 32 volume levels. The LSB represents 1.5 dB, and the gain range is +12 dB to −34.5 dB. The default value is 0 dB, mute enabled.
RM	Right-Channel Mute	Once enabled by the MSPLT bit in Register 0x76, this bit mutes the right channel separately from the AM bit. Otherwise, this bit always reads 0 and has no affect when set to 1.
LAV [4:0]	Left AUX Volume	Allows setting the AUX left-channel attenuator in 32 volume levels. The LSB represents 1.5 dB, and the gain range is +12 dB to −34.5 dB. The default value is 0 dB, mute enabled.
AM	AUX Volume Mute	When this bit is set to 1, both the left and right channels are muted, unless the MSPLT bit in Register 0x76 is set to 1, in which case this mute bit affects only the left channel.

PCM-OUT VOLUME REGISTER
Index 0x18

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x18	PCM-Out Volume	OM	X	X	LOV4	LOV3	LOV2	LOV1	LOV0	RM[1]	X	X	ROV4	ROV3	ROV2	ROV1	ROV0	0x8808

[1] For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 0x76. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, the RM bit has no effect.
All registers are not shown, and bits containing an X are assumed to be reserved. Refer to Table 22 for examples.

Table 21.

Bit	Mnemonic	Function
ROV [4:0]	Right PCM-Out Volume	Allows setting the PCM right-channel attenuator in 32 volume levels. The LSB represents 1.5 dB, and the range is +12 dB to −34.5 dB. The default value is 0 dB, mute enabled.
RM	Right-Channel Mute	Once enabled by the MSPLT bit in Register 0x76, this bit mutes the right channel separately from the OM bit. Otherwise, this bit always reads 0 and has no effect when set to 1.
LOV [4:0]	Left PCM-Out Volume	Allows setting the PCM left-channel attenuator in 32 volume levels. The LSB represents 1.5 dB, and the range is +12 dB to −34.5 dB. The default value is 0 dB, mute enabled.
OM	PCM-Out Volume Mute	When this bit is set to 1, both the left and right channels are muted unless the MSPLT bit in Register 0x76 is set to 1, in which case this mute bit affects only the left channel.

Table 22. Volume Settings for Line-In, CD Volume, AUX, and PCM-Out

Reg. 0x76	Control Bits							
	Line-In (0x10), CD (0x12), AUX (0x16), and PCM-Out (0x18)							
	Left-Channel Volume D [12:8]				Right-Channel Volume D [4:0]			
MSPLT[1]	D15	Write	Readback	Function	D7[1]	Write	Readback	Function
0	0	0 0000	0 0000	12 dB Gain	X	0 0000	0 0000	12 dB Gain
0	0	0 1000	0 1000	0 dB Gain	X	0 1000	0 1000	0 dB Gain
0	0	1 1111	1 1111	+34.5 dB Gain	X	1 1111	1 1111	−34.5 dB Gain
0	1	X XXXX	X XXXX	−∞ dB Gain, Muted	X	X XXXX	X XXXX	−∞ dB Gain, Muted
1	0	1 1111	1 1111	−34.5 dB Gain	1	X XXXX	X XXXX	−∞ dB Gain, Right Only Muted
1	1	X XXXX	X XXXX	−∞ dB Gain, Left Only Muted	0	1 1111	1 1111	−34.5 dB Gain
1	1	X XXXX	X XXXX	−∞ dB Gain, Left Muted	1	X XXXX	X XXXX	−∞ dB Gain, Right Muted

[1] For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 0x76. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, the RM bit has no effect.
X is a wild card, and has no effect on the value.

RECORD SELECT CONTROL REGISTER
Index 0x1A

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x1A	Record Select	X	X	X	X	X	LS2	LS1	LS0	X	X	X	X	X	RS2	RS1	RS0	0x0000

Used to select the record source independently for right and left. The default value is 0x0000, which corresponds to MIC In. Refer to Table 24 for examples.
All registers are not shown, and bits containing an X are assumed to be reserved.

Table 23.

Bit	Function
RS [2:0]	Right Record Select
LS [2:0]	Left Record Select

Table 24. Settings for Record Select Control

LS [10:8]	Left Record Source	RS [2:0]	Right Record Source
000	MIC	000	MIC
001	CD_L	001	CD_R
010	Muted	010	Muted
011	AUX_L	011	AUX_R
100	LINE_IN_L	100	LINE_IN_R
101	Stereo Mix (L)	101	Stereo Mix (R)
110	Mono Mix	110	Mono Mix
111	PHONE_IN	111	PHONE_IN

RECORD GAIN REGISTER
Index 0x1C

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x1C	Record Gain	IM	X	X	X	LIM3	LIM2	LIM1	LIM0	RM[1]	X	X	X	RIM3	RIM2	RIM1	RIM0	0x8000

[1] For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 0x76. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, the RM bit has no effect.
All registers are not shown, and bits containing an X are assumed to be reserved. Refer to Table 24 for examples.

Table 25.

Bit	Mnemonic	Function
RIM [3:0]	Right Input Mixer Gain Control	Each LSB represents 1.5 dB, 0000 = 0 dB, and the gain range is 0 dB to 22.5 dB.
RM	Right-Channel Mute	Once enabled by the MSPLT bit in Register 0x76, this bit mutes the right channel separately from the IM bit. Otherwise, this bit always reads 0 and has no affect when set to 1.
LIM [3:0]	Left Input Mixer Gain Control	Each LSB represents 1.5 dB, 0000 = 0 dB, and the gain range is 0 dB to 22.5 dB.
IM	Input Mute	When this bit is set to 1, both the left and right channels are muted, unless the MSPLT bit in Register 0x76 is set to 1, in which case this mute bit affects only the left channel.

Table 26. Settings for Record Gain Register

Reg. 0x76	Control Bits Record Gain (1Channel)							
	Left-Channel Input Mixer D [11:8]				Right-Channel Input Mixer D [3:0]			
MSPLT[1]	D15	Write	Readback	Function	D7[1]	Write	Readback	Function
0	0	1111	1111	22.5 dB Gain	X	1111	1111	22.5 dB Gain
0	0	0000	0000	0 dB Gain	X	0000	0000	0 dB Gain
0	1	XXXX	XXXX	−∞ dB Gain, Muted	X	XXXX	XXXX	−∞ dB Gain, Muted
1	0	1111	1111	22.5 dB Gain	1	XXXX	XXXX	−∞ dB Gain, Right Only Muted
1	1	XXXX	XXXX	−∞ dB Gain, Left Only Muted	0	1111	1111	22.5 dB Gain
1	1	XXXX	XXXX	−∞ dB Gain, Left Muted	1	XXXX	XXXX	−∞ dB Gain, Right Muted

[1] For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 0x76. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, the RM bit has no effect.
X is a wild card, and has no effect on the value.

GENERAL-PURPOSE REGISTER

Index 0x20

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x20	General-Purpose	X	X	X	X	X	X	MIX	MS	LPBK	X	X	X	X	X	X	X	0x0000

This register should be read before writing to generate a mask for only the bit(s) that need to be changed.
All registers are not shown, and bits containing an X are assumed to be reserved.

Table 27.

Bit	Mnemonic	Function
LPBK	Loopback Control	ADC/DAC Digital Loopback Mode. 0 = No Loopback (default). 1 = Loopback PCM Digital Data from ADC Output to DAC.
MS	MIC Select	Selects mono MIC input. 0 = Select MIC1. 1 = Select MIC2. See the 2CMIC bit in Register 0x76 to enable stereo microphone recording.
MIX	Mono Output Select	Selects mono output audio source. 0 = Mixer Mono Output (reset default). 1 = MIC1 Channel.

POWER-DOWN CONTROL/STATUS REGISTER

Index 0x26

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x26	Power-Down Ctrl/Stat	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	0x000X

The ready bits are read-only; writing to REF, ANL, DAC, ADC has no effect. These bits indicate the status for the AD1981BL subsections. If the bit is a 1, that subsection is ready. Ready is defined as the subsection able to perform in its nominal state.
All registers are not shown, and bits containing an X are assumed to be reserved.

Table 28.

Bit	Mnemonic	Function
ADC		ADC Sections Ready to Transmit Data.
DAC		DAC Sections Ready to Accept Data.
ANL		Analog Amplifiers, Attenuators, and Mixers Ready.
REF		Voltage References, V_{REF} and V_{REFOUT}, Up to Nominal Level.
PR [6:0]	Codec Power-Down Modes	The first three bits are to be used individually rather than in combination with each other. PR3 can be used in combination with PR2 or by itself. The mixer and reference cannot be powered down via PR3 unless the ADCs and DACs are also powered down.
		Nothing else can be powered up until the reference is powered up. PR5 has no effect unless all ADCs, DACs, and the ac-link are powered down. The reference and the mixer can be either powered up or powered down, but all power-up sequences must be allowed to run to completion before PR5 and PR4 are both set.
		In multiple codec systems, the master codec's PR5 and PR4 bits control the slave codec. PR5 is also effective in the slave codec, if the master's PR5 bit is clear, but the PR4 bit has no effect except to enable or disable PR5.
EAPD	External Audio Power-Down Control	Controls the state of the EAPD pin.
		EAPD = 0 sets the EAPD pin low, enabling an external power amplifier (reset default).
		EAPD = 1 sets the EAPD pin high, shutting the external power amplifier off.

Table 29.

Power-Down State	Set Bits	PR [6:0]
ADCs and Input MUX Power-Down	PR0	[000 0001]
DACs Power-Down	PR1	[000 0010]
Analog Mixer Power-Down (V_{REF} and V_{REFOUT} On)	PR1, PR2	[000 0101]
Analog Mixer Power-Down (V_{REF} and V_{REFOUT} Off)	PR0, PR1, PR3	[000 1011]
AC-Link Interface Power-Down	PR4	[001 0000]
Internal Clocks Disabled	PR0, PR1, PR4, PR5	[011 0011]
ADC and DAC Power-Down	PR0, PR1	[000 0011]
V_{REF} Standby Mode	PR0, PR1, PR2, PR4, PR5	[011 0111]
Total Power-Down	PR0, PR1, PR2, PR3, PR4, PR5, PR6	[111 1111]
Headphone Amp Power-In Standby	PR6	[100 0000]

EXTENDED AUDIO ID REGISTER

Index 0x28

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x28	Ext'd Audio ID	IDC1	IDC0	X	X	REVC1	REVC0	AMAP	X	X	X	DSA1	DSA0	X	SPDIF	X	VRAS	0xX605

The extended audio ID register identifies which extended audio features are supported. A nonzero extended audio ID value indicates that one or more of the extended audio features are supported.
All registers are not shown, and bits containing an X are assumed to be reserved.

Table 30.

Bit	Mnemonic	Function
VRAS	Variable Rate PCM Audio Support (Read-Only)	This bit returns a 1 when Read To indicates that the variable rate PCM audio is supported.
SPDIF	SPDIF Support (Read-Only)	This bit returns a 1 when Read To indicates that the SPDIF transmitter is supported (IEC958). This bit is also used to validate that the SPDIF transmitter output is enabled. The SPDIF bit can be set high only if the SPDIF pin (Pin 48) is pulled down at power-up, enabling the codec transmitter logic. If the SPDIF pin is floating or pulled high at power-up, the transmitter logic is disabled; therefore, this bit returns a low, indicating that the SPDIF transmitter is not available. This bit must always be read back to verify that the SPDIF transmitter is actually enabled.
DSA [1:0]	DAC Slot Assignments (Read/Write)	Reset default = 00. 00 DACs 1, 2 = 3 and 4. 01 DACs 1, 2 = 7 and 8. 10 DACs 1, 2 = 6 and 9. 11 Reserved.
AMAP	Slot DAC Mappings Based on Codec ID (Read-Only)	This bit returns a 1 when read to indicate that slot/DAC mappings based on the codec ID are supported.
REVC [1:0]	AC '97 Revision Compliance	REVC [1:0] = 01 indicates that the codec is AC '97 revision 2.2-compliant (read-only).
IDC [1:0]	Indicates Codec Configuration (Read-Only)	00 = Primary. 01, 10, 11 = Secondary.

EXTENDED AUDIO STATUS AND CONTROL REGISTER

Index 0x2A

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x2A	Ext'd Audio Stat/Ctrl	VFORCE	X	X	X	X	SPCV	X	X	X	X	SPSA1	SPSA0	X	SPDIF	X	VRA	0x0000

The extended audio status and control register is a read/write register that provides status and control of the extended audio features.
All registers are not shown, and bits containing an X are assumed to be reserved.

Table 31.

Bit	Mnemonic	Function
VRA	Variable Rate Audio (Read/Write)	VRA = 0 sets the fixed sample rate audio to 48 kHz (reset default). VRA = 1 enables variable rate audio mode (enables sample rate registers and SLOTREQ signaling).
SPDIF	SPDIF Transmitter Subsystem Enable/Disable Bit (Read/Write)	SPDIF = 1 enables the SPDIF transmitter. SPDIF = 0 disables the SPDIF transmitter (default). This bit is also used to validate that the SPDIF transmitter output is enabled. The SPDIF bit can be set high only if the SPDIF pin (Pin 48) is pulled down at power-up, enabling the codec transmitter logic. If the SPDIF pin is floating or pulled high at power-up, the transmitter logic is disabled and this bit returns a low, indicating that the SPDIF transmitter is not available. This bit must always be read back to verify that the SPDIF transmitter is enabled.
SPSA [1:0]	SPDIF Slot Assignment Bits (Read/Write)	These bits control the SPDIF slot assignment and respective defaults, depending on the codec ID configuration.

Bit	Mnemonic	Function
SPCV	SPDIF Configuration Valid (Read-Only)	This bit indicates the status of the SPDIF transmitter subsystem, enabling the driver to determine if the currently programmed SPDIF configuration is supported. SPCV is always valid, independent of the SPDIF enable bit status. SPCV = 0 indicates that the current SPDIF configuration (SPSA, SPSR, DAC slot rate, DRS) is not valid (not supported). SPCV = 1 indicates that the current SPDIF configuration (SPSA, SPSR, DAC slot rate, DRS) is valid (supported).
VFORCE	Validity Force Bit (Reset Default = 0)	When asserted, this bit forces the SPDIF stream validity flag (Bit 28 within each SPDIF L/R subframe) to be controlled by the V bit (D15) in Register 0x3A (SPDIF control register). VFORCE = 0 and V = 0; the validity bit is managed by the codec error detection logic. VFORCE = 0 and V = 1; the validity bit is forced high, indicating the subframe data is invalid. VFORCE = 1 and V = 0; the validity bit is forced low, indicating the subframe data is valid. VFORCE = 1 and V = 1; the validity bit is forced high, indicating the subframe data is invalid.

Table 32. AC '97 2.2 AMAP-Compliant Default SPDIF Slot Assignments

Codec ID	Function	SPSA = 00	SPSA = 01	SPSA = 10	SPSA = 11
00	2-Channel Primary w/SPDIF	3 and 4	7 and 8 (default)	6 and 9	10 and 11
00	4-Channel Primary w/SPDIF	3 and 4	7 and 8	6 and 9 (default)	10 and 11
00	6-Channel Primary w/SPDIF	3 and 4	7 and 8	6 and 9	10 and 11 (default)
01	+2-Channel Secondary w/SPDIF	3 and 4	7 and 8	6 and 9 (default)	
01	+4-Channel Secondary w/SPDIF	3 and 4	7 and 8	6 and 9	10 and 11 (default)
10	+2-Channel Secondary w/SPDIF	3 and 4	7 and 8	6 and 9 (default)	
10	+4-Channel Secondary w/SPDIF	3 and 4	7 and 8	6 and 9	10 and 11 (default)
11	+2-Channel Secondary w/SPDIF	3 and 4	7 and 8	6 and 9	10 and 11 (default)

PCM FRONT DAC RATE REGISTER

Index 0x2C

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x2C	PCM Front DAC Rate	SRF15	SRF14	SRF13	SRF12	SRF11	SRF10	SRF9	SRF8	SRF7	SRF6	SRF5	SRF4	SRF3	SRF2	SRF1	SRF0	0xBB80

This read/write sample rate control register contains a 16-bit unsigned value, representing the rate of operation in Hz.

Table 33.

Bit	Mnemonic	Function
SRF [15:0]	Sample Rate	The sampling frequency range is from 7 kHz (0x1B58) to 48 kHz (0xBB80) in 1 Hz increments. If 0 is written to VRA, the sample rate is reset to 48 kHz.

PCM ADC RATE REGISTER

Index 0x32

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x32	PCM L/R ADC Rate	SRA15	SRA14	SRA13	SRA12	SRA11	SRA10	SRA9	SRA8	SRA7	SRA6	SRA5	SRA4	SRA3	SRA2	SRA1	SRA0	0xBB80

This read/write sample rate control register contains a 16-bit unsigned value, representing the rate of operation in Hz.

Table 34.

Bit	Mnemonic	Function
SRA [15:0]	Sample Rate	The sampling frequency range is from 7 kHz (0x1B58) to 48 kHz (0xBB80) in 1 Hz increments. If 0 is written to VRA, the sample rate is reset to 48 kHz.

SPDIF CONTROL REGISTER
Index 0x3A

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x3A	SPDIF Control	V	X	SPSR1	SPSR0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	$\overline{\text{AUD}}$	PRO	0x2000

Register 0x3A is a read/write register that controls SPDIF functionality and manages bit fields propagated as channel status (or subframe in the V case). With the exception of V, this register should be written to only when the SPDIF transmitter is disabled (SPDIF bit in Register 0x2A is 0). This ensures that control and status information start up correctly at the beginning of SPDIF transmission.

Table 35.

Bit	Mnemonic	Function
PRO	Professional	1 = Professional use of channel status. 0 = Consumer.
$\overline{\text{AUD}}$	Nonaudio	1 = Data is non-PCM format. 0 = Data is PCM format.
COPY	Copyright	1 = Copyright is asserted. 0 = Copyright is not asserted.
PRE	Pre-emphasis	1 = Filter pre-emphasis is 50 µs/15 µs. 0 = Pre-emphasis is none.
CC [6:0]	Category Code	Programmed according to IEC standards, or as appropriate.
L	Generation Level	Programmed according to IEC standards, or as appropriate.
SPSR [1:0]	SPDIF Transmit Sample Rate	SPSR [1:0] = 00: Transmit sample rate is 44.1 kHz. SPSR [1:0] = 01: Reserved. SPSR [1:0] = 10: Transmit sample rate is 48 kHz (reset default). SPSR [1:0] = 11: Not supported.
V	Validity	This bit affects the validity flag (Bit 28 transmitted in each SPDIF L/R subframe) and enables the SPDIF transmitter to maintain connection during error or mute conditions. V = 1: Each SPDIF subframe (L + R) has Bit 28 set to 1. This tags both samples as invalid. V = 0: Each SPDIF subframe (L + R) has Bit 28 set to 0 for valid data and 1 for invalid data (error condition). When V = 0, asserting the VFORCE bit (D15) in Register 0x2A (Ext'd Audio Stat/Ctrl) forces the validity flag low, marking both samples as valid.

EQ CONTROL REGISTER
Index 0x60

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x60	EQ Ctrl	EQM	MAD LBEN	X	X	X	X	X	X	SYM	CHS	BCA5	BCA4	BCA3	BCA2	BCA1	BCA0	0x8080

Register 0x60 is a read/write register that controls the equalizer functionality and data setup. This register contains the biquad and coefficient address pointer, which is used in conjunction with the EQ data register (0x78) to set up the equalizer coefficients. The reset default disables the equalizer function until the coefficients can be properly set up by the software and sets the symmetry bit to allow equal coefficients for left and right channels.
All registers are not shown, and bits containing an X are assumed to be reserved.

Table 36.

Bit	Mnemonic	Function
BCA [5:0]	Biquad and Coefficient Address Pointer	biquad 0 coef a0 BCA[5:0] = 011011 biquad 0 coef a1 BCA[5:0] = 011010 biquad 0 coef a2 BCA[5:0] = 011001 biquad 0 coef b1 BCA[5:0] = 011101 biquad 0 coef b2 BCA[5:0] = 011100 biquad 1 coef a0 BCA[5:0] = 100000 biquad 1 coef a1 BCA[5:0] = 011111

Bit	Mnemonic	Function
		biquad 1 coef a2 BCA[5:0] = 011110 biquad 1 coef b1 BCA[5:0] = 100010 biquad 1 coef b2 BCA[5:0] = 100001 biquad 2 coef a0 BCA[5:0] = 100101 biquad 2 coef a1 BCA[5:0] = 100100 biquad 2 coef a2 BCA[5:0] = 100011 biquad 2 coef b1 BCA[5:0] = 100111 biquad 2 coef b2 BCA[5:0] = 100110 biquad 3 coef a0 BCA[5:0] = 101010 biquad 3 coef a1 BCA[5:0] = 101001 biquad 3 coef a2 BCA[5:0] = 101000 biquad 3 coef b1 BCA[5:0] = 101100 biquad 3 coef b2 BCA[5:0] = 101011 biquad 4 coef a0 BCA[5:0] = 101111 biquad 4 coef a1 BCA[5:0] = 101110 biquad 4 coef a2 BCA[5:0] = 101101 biquad 4 coef b1 BCA[5:0] = 110001 biquad 4 coef b2 BCA[5:0] = 110000 biquad 5 coef a0 BCA[5:0] = 110100 biquad 5 coef a1 BCA[5:0] = 110011 biquad 5 coef a2 BCA[5:0] = 110010 biquad 5 coef b1 BCA[5:0] = 110110 biquad 5 coef b2 BCA[5:0] = 110101 biquad 6 coef a0 BCA[5:0] = 111001 biquad 6 coef a1 BCA[5:0] = 111000 biquad 6 coef a2 BCA[5:0] = 110111 biquad 6 coef b1 BCA[5:0] = 111011 biquad 6 coef b2 BCA[5:0] = 111010
CHS	Channel Select	CHS = 0 selects the left-channel coefficient's data block. CHS = 1 selects the right-channel coefficient's data block.
SYM	Symmetry	When set to 1, this bit indicates that the left- and right-channel coefficients are equal. This shortens the coefficients' setup sequence, because only the left-channel coefficients need to be addressed and set up. The right-channel coefficients are fetched from the left-channel memory.
MAD LBEN	Mixer ADC Loopback Enable	Enables mixer ADC data to be summed into the PCM stream. 0 = No loopback allowed (default). 1 = Enable loopback.
EQM	Equalizer Mute	When set to 1, this bit disables the equalizer function (allows all data to pass through). The reset default sets this bit to 1, disabling the equalizer function until the biquad coefficients can be properly set.

EQ DATA REGISTER
Index 0x62

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x62	EQ Data	CFD15	CFD14	CFD13	CFD12	CFD11	CFD10	CFD9	CFD8	CFD7	CFD6	CFD5	CFD4	CFD3	CFD2	CFD1	CFD0	0x0000

This read/write register is used to transfer EQ biquad coefficients into memory. The register data is transferred to, or retrieved from, the address pointed to by the BCA bits in the EQ Cntrl Register (0x60). Data is written to memory only if the EQM bit (Register 0x60, Bit 15) is asserted.

Table 37.

Bit	Mnemonic	Function
CFD [15:0]	Coefficient Data	The biquad coefficients are fixed-point format values with 16 bits of resolution. The CFD15 bit is the MSB, and the CFD0 bit is the LSB.

MIXER ADC, INPUT GAIN REGISTER
Index 0x64

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x64	Mixer ADC, Volume	MXM	X	X	X	LMG3	LMG2	LMG1	LMG0	RM[1]	X	X	X	RMG3	RMG2	RMG1	RMG0	0x8000

[1] For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 0x76. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, the RM bit has no effect.
All registers are not shown, and bits containing an X are assumed to be reserved. Refer to Table 39 for examples.

Table 38.

Bit	Mnemonic	Function
RMG [3:0]	Right Mixer Gain Control	This register controls the gain into the mixer ADC from 0 dB to a maximum gain of 22.5 dB. The least significant bit represents 1.5 dB.
RM	Right-Channel Mute	Once enabled by the MSPLT bit in Register 0x76, this bit mutes the right channel separately from the MXM bit. Otherwise, this bit always reads 0 and has no affect when set to 1.
LMG [3:0]	Left Mixer Gain Control	This register controls the gain into the mixer ADC, from 0 dB to a maximum gain of 22.5 dB. The least significant bit represents 1.5 dB.
MXM	Mixer Gain Register Mute	0 = Unmuted. 1 = Muted (reset default).

Table 39. Settings for Mixer ADC, Input Gain

Reg. 0x76	Control Bits Mixer ADC, Input Gain (0x64)							
	Left-Channel Mixer Gain D [11:8]				Right-Channel Mixer Gain D [3:0]			
MSPLT[1]	D15	Write	Readback	Function	D7[1]	Write	Readback	Function
0	0	1111	1111	22.5 dB Gain	X	1111	1111	22.5 dB Gain
0	0	0000	0000	0 dB Gain	X	0000	0000	0 dB Gain
0	1	XXXX	XXXX	−∞ dB Gain, Muted	X	XXXX	XXXX	−∞ dB Gain, Muted
1	0	1111	1111	22.5 dB Gain	1	XXXX	XXXX	−∞ dB Gain, Right Only Muted
1	1	XXXX	XXXX	−∞ dB Gain, Left Only Muted	0	1111	1111	22.5 dB Gain
1	1	XXXX	XXXX	−∞ dB Gain, Left Muted	1	XXXX	XXXX	−∞ dB Gain, Right Muted

[1] For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 0x76. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, the RM bit has no effect.
X is a wild card, and has no effect on the value.

JACK SENSE/AUDIO INTERRUPT/STATUS REGISTER

Index 0x72

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x72	Jack Sense	X	X	X	JS MT2	JS MT1	JS MT0	JS1 EQB	JS0 EQB	JS1 TMR	JS0 TMR	JS1 MD	JS0 MD	JS1 ST	JS0 ST	JS1 INT	JS0 INT	0x0000

All register bits are read/write except for JS0ST and JS1ST, which are read-only.
All registers are not shown, and bits containing an X are assumed to be reserved.

Table 40.

Bit	Mnemonic	Function
JS0INT	JS0 Interrupt	This bit indicates that Pin JS0 has generated an interrupt. This bit remains set until the software services the JS0 interrupt, that is, JS0 ISR should clear this bit by writing a 0 to it. The interrupt to the system is an OR combination of this bit and JS1INT. The actual interrupt implementation is selected by the INTS bit (Register 0x76). It is also possible to generate a software system interrupt by writing a 1 to this bit.
JS1INT	JS1 Interrupt	This bit indicates that Pin JS1 has generated an interrupt. This bit remains set until the software services the JS1 interrupt, that is, JS1 ISR should clear this bit by writing a 0 to it. See the JS0INT description for details.
JS0ST	JS0 State	This bit always reports the logic state of the JS0 pin.
JS1ST	JS1 State	This bit always reports the logic state of the JS1 pin.
JS0MD	JS0 Mode	This bit selects the operation mode for the JS0 pin. 0 = Jack sense mode (default). 1 = Interrupt mode.
JS1MD	JS1 Mode	This bit selects the operation mode for the JS1 pin. 0 = Jack sense mode (default). 1 = Interrupt mode.
JS0TMR	JS0 Timer Enable	If this bit is set to 1, JS0 must be high for >278 ms to be recognized.
JS1TMR	JS1 Timer Enable	If this bit is set to 1, JS1 must be high for >278 ms to be recognized.
JS0EQB	JS0 EQ Bypass Enable	This bit enables JS0 to control the EQ bypass. When this bit is set to 1, JS0 = 1 causes the EQ to be bypassed.
JS1EQB	JS1 EQ Bypass Enable	This bit enables JS1 to control the EQ bypass. When this bit is set to 1, JS1 = 1 causes the EQ to be bypassed.
JSMT [2:0]	JS Mute Enable Selector	These three bits select and enable the jack sense muting action (see Table 41).

Table 41. Jack Sense Mute Select—JSMT [2:0]

Ref	JS1 Headphone	JS0 LINE_OUT	JSMT2	JSMT1	JSMT0	HP_OUT	LINE_OUT	MONO_OUT	Notes
0	OUT (0)	OUT (0)	0	0	0	ACTIVE	ACTIVE	ACTIVE	JS0 and JS1 ignored.
1	OUT (0)	IN (1)	0	0	0	ACTIVE	ACTIVE	ACTIVE	
2	IN (1)	OUT (0)	0	0	0	ACTIVE	ACTIVE	ACTIVE	
3	IN (1)	IN (1)	0	0	0	ACTIVE	ACTIVE	ACTIVE	
4	OUT (0)	OUT (0)	0	0	1	FMUTE	FMUTE	ACTIVE	JS0 no mute action; JS1 mutes Line_Out.
5	OUT (0)	IN (1)	0	0	1	FMUTE	ACTIVE	ACTIVE	
6	IN (1)	OUT (0)	0	0	1	ACTIVE	FMUTE	ACTIVE	
7	IN (1)	IN (1)	0	0	1	ACTIVE	FMUTE	ACTIVE	
8	OUT (0)	OUT (0)	0	1	0	FMUTE	FMUTE	ACTIVE	JS0 no mute action; JS1 mutes Mono and Line-Out.
9	OUT (0)	IN (1)	0	1	0	FMUTE	ACTIVE	ACTIVE	
10	IN (1)	OUT (0)	0	1	0	ACTIVE	FMUTE	FMUTE	
11	IN (1)	IN (1)	0	1	0	ACTIVE	FMUTE	FMUTE	
12	OUT (0)	OUT (0)	0	1	1	**	**	**	** Reserved.
13	OUT (0)	IN (1)	0	1	1	**	**	**	
14	IN (1)	OUT (0)	0	1	1	**	**	**	
15	IN (1)	IN (1)	0	1	1	**	**	**	
16	OUT (0)	OUT (0)	1	0	0	FMUTE	FMUTE	ACTIVE	JS0 mutes Mono; JS1 no mute action.
17	OUT (0)	IN (1)	1	0	0	FMUTE	ACTIVE	FMUTE	
18	IN (1)	OUT (0)	1	0	0	ACTIVE	FMUTE	ACTIVE	
19	IN (1)	IN (1)	1	0	0	ACTIVE	ACTIVE	FMUTE	
20	OUT (0)	OUT (0)	1	0	1	FMUTE	FMUTE	ACTIVE	JS0 mutes Mono; JS1 mutes Line-Out.
21	OUT (0)	IN (1)	1	0	1	FMUTE	ACTIVE	FMUTE	
22	IN (1)	OUT (0)	1	0	1	ACTIVE	FMUTE	ACTIVE	
23	IN (1)	IN (1)	1	0	1	ACTIVE	FMUTE	FMUTE	
24	OUT (0)	OUT (0)	1	1	0	FMUTE	FMUTE	ACTIVE	JS0 mutes Mono; JS1 mutes Mono and Line-Out.
25	OUT (0)	IN (1)	1	1	0	FMUTE	ACTIVE	FMUTE	
26	IN (1)	OUT (0)	1	1	0	ACTIVE	FMUTE	FMUTE	
27	IN (1)	IN (1)	1	1	0	ACTIVE	FMUTE	FMUTE	
28	OUT (0)	OUT (0)	1	1	1	**	**	**	** Reserved.
29	OUT (0)	IN (1)	1	1	1	**	**	**	
30	IN (1)	OUT (0)	1	1	1	**	**	**	
31	IN (1)	IN (1)	1	1	1	**	**	**	

FMUTE = Output is forced to mute independent of the respective volume register setting.
ACTIVE = Output is not muted, and its status is dependent on the respective volume register setting.
OUT = Nothing plugged into the jack and, therefore, the JS status is low (via the load resistor pull-down).
IN = Jack has plug inserted and, therefore, the JS status is high (via the codec JS internal pull-up).

SERIAL CONFIGURATION REGISTER
Index 0x74

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x74	Serial Config	SLOT16	REGM2	REGM1	REGM0	X	X	X	CHEN	X	X	X	INTS	X	SPAL	SPDZ	SPLNK	0x7001

This register is not reset when the reset register (Register 0x00) is written.
All registers are not shown, and bits containing an X are assumed to be reserved.

Table 42.

Bit	Mnemonic	Function
SPLNK	SPDIF Link	This bit enables the SPDIF to link with the DAC for data requests. 0 = SPDIF and DAC are not linked. 1 = SPDIF and DAC are linked and receive the same data requests (reset default).
SPDZ	SPDIF DACZ	0 = Repeat last sample out of the SPDIF stream if FIFO underruns (reset default). 1 = Forces midscale sample out the SPDIF stream if FIFO underruns.
SPAL	SPDIF ADC Loop-Around	0 = SPDIF transmitter is connected to the ac-link stream (reset default). 1 = SPDIF transmitter is connected to the digital ADC stream, not the ac-link.
INTS	Interrupt Mode Select	This bit selects the JS interrupt implementation path. 0 = Bit 0 Slot 12 (modem interrupt). 1 = Slot 6 valid bit (MIC ADC interrupt).
CHEN	Chain Enable	This bit enables chaining of a slave codec SDATA_IN stream into the $\overline{ID0}$ pin (Pin 45). 0 = Disable chaining (reset default). 1 = Enable chaining into $\overline{ID0}$ pin.
REGM0	Master Codec Register Mask	
REGM1	Slave 1 Codec Register Mask	
REGM2	Slave 2 Codec Register Mask	
SLOT16	Enable 16-Bit Slot Mode	Slot 16 makes all ac-link slots 16 bits in length, formatted into 16 slots. This is a preferred mode for DSP serial port interfacing.

MISCELLANEOUS CONTROL BIT REGISTER
Index 0x76

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x76	Misc Control Bit	DACZ	X	MSPLT	LODIS	DAM	X	FMXE	X	MADPD	2CMIC	X	MADST	VREFH	VREFD	MBG1	MBG0	0x0000

All registers are not shown, and bits containing an X are assumed to be reserved.

Table 43.

Bit	Mnemonic	Function
MBG [1:0]	MIC Boost Gain Change Register	These two bits allow changing the MIC preamp gain from the nominal 20 dB gain. This gain setting takes effect only while Bit D6 (M20) on the MIC volume register (0x0E) is set to 1; otherwise, the MIC boost block has a gain of 0 dB. 00 = 20 dB gain (reset default). 01 = 10 dB gain. 10 = 30 dB gain. 11 = Reserved.

Bit	Mnemonic	Function
VREFD	V_{REFOUT} Disable	This bit disables V_{REFOUT}, placing it into high Z out mode. This bit overrides the VREFH bit selection. 0 = V_{REFOUT} pin is driven by the internal reference (reset default). 1 = V_{REFOUT} pin is placed into high Z out mode.
VREFH	V_{REFOUT} High	0 = V_{REFOUT} pin is set to 2.25 V output (reset default). 1 = V_{REFOUT} pin is set to 2.25 V output (is set to 3.7 V only if AVDD = 5 V).
MADST	Mixer ADC Status Bit	This bit indicates status of the mixer digitizing ADC (left and right channels). 0 = Mixer ADC not ready. 1 = Mixer ADC ready.
2CMIC	2-Channel MIC Select	This bit enables simultaneous recording from MIC1 and MIC2 inputs for applications that use a stereo microphone array. This register works in conjunction with the MS bit in Register 0x20. 0 = MIC1 or MIC2 (determined by the MS bit) is routed to the record selector's left and right MIC channels, as well as to the mixer (reset default). 1 = MIC1 is routed to the record selector's left MIC channel and MIC2 is routed to the record selector's right MIC channel. In this mode, the MS bit should be set low, and MIC1 can still be enabled into the mixer.
MADPD	Mixer ADC Power-Down	This bit controls power-down for mixer digitizing ADC. 0 = Mixer ADC is powered on (default). 1 = Mixer ADC is powered down.
FMXE	Front DAC into Mixer Enable	This bit controls the front (main) DAC to mixer mute switches. 0 = Front DAC outputs are allowed to sum into the mixer (reset default). 1 = Front DAC outputs are muted into the mixer (blocked).
DAM	Digital Audio Mode	PCM DAC outputs bypass the analog mixer and are sent directly to the codec output.
LODIS	LINE_OUT Disable	This bit disables the LINE_OUT pins (L/R), placing them into high Z mode so that the assigned output audio jack can be shared for the input function (or other function). 0 = LINE_OUT pins have normal audio drive capability (reset default). 1 = LINE_OUT pins are placed into high Z mode.
MSPLT	Mute Split	This bit allows separate mute control bits for the master, headphone, LINE_IN, CD, AUX, and PCM volume control registers as well as for the record gain register. 0 = Both left- and right-channel mutes are controlled by Bit 15 in the respective registers (reset default). 1 = Bit 15 affects only the left-channel mute, and Bit 7 affects only the right-channel mute.
DACZ	DAC Zero-Fill	This bit determines DAC data fill under starved conditions. 0 = DAC data is repeated when DACs are starved for data (reset default). 1 = DAC is zero-filled when DACs are starved for data.

VENDOR ID REGISTERS

Index 0x7C–0x7E

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x7C	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	0x4144

S[7:0] This register is ASCII encoded to A.

F[7:0] This register is ASCII encoded to D.

Reg No.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x7E	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	0x5374

T[7:0] This register is ASCII encoded to S.

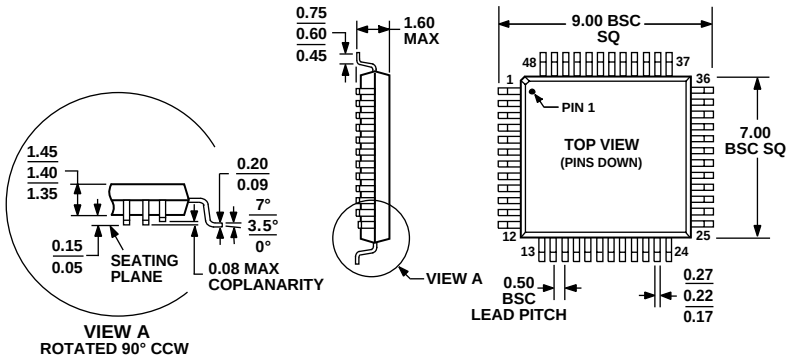
REV[7:0] Vendor-specific revision number: The AD1981BL assigns 0x74 to this field.

Table 44. Codec ID and External Clock Selection

$\overline{ID1}$	$\overline{ID0}$	Codec ID	Codec Clocking Source	
1	1	(00) Primary	24.576 MHz	Local crystal or external into XTL_IN.
1	0	(01) Secondary	12.288 MHz	External into BIT_CLK.
0	1	(00) Primary	48.000 MHz	External into XTL_IN.
0	0	(00) Primary	14.31818 MHz	External into XTL_IN.

Internally, the $\overline{ID}$ pins have weak pull-ups and are inverted.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026BBC

Figure 10. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1981BLJST	0°C to 70°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
AD1981BLJST-REEL	0°C to 70°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
AD1981BLJSTZ[1]	0°C to 70°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
AD1981BLJSTZ-REEL[1]	0°C to 70°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48

[1]Z = Pb-free part. The AD1981BLJSTZ is a lead-free environmentally friendly product. It is manufactured using the most up-to-date materials and processes. The coating on the leads of each device is 100% pure tin electroplate. The device is suitable for lead-free applications and can withstand surface-mount soldering at up to 255°C (±5°C). In addition, it is backward compatible with conventional tin-lead soldering processes. This means that the electroplated tin coating can be soldered with tin-lead solder pastes at reflow temperatures of 220°C to 235°C.

D04321–0–1/05(A)